REMARKS

This paper is responsive to the Office Action dated September 24, 2004. All rejections and objections of the Examiner are respectfully traversed. Reconsideration and further examination are respectfully requested.

At paragraphs 2-3 of the Office Action, the Examiner rejected independent claims 1 and 6 for obviousness under 35 U.S.C. 103, citing United States patent number 6,499,099 of Cho ("Cho"). Applicants respectfully traverse this rejection.

Cho discloses a central processing unit having an extension instruction including a memory address, an offset and a fixed length instruction of varying immediate data. The central processing unit of Cho includes a general register, a special register, a register file constituted as an inner register, a function block for executing the calculation function, an instruction register for storing the instruction, a control block for generating and outputting a control signal to the instruction register and a plurality of status flags. The special register of Cho enables access by a programmer, and includes an extension data field for storing extension data, or an extension register having the extension data field as one element and an extension flag for changing its status when the instruction having the extension data in the extension register is executed, and including one or a plurality of bits that is accessible to a programmer.

Nowhere in Cho is there disclosed or suggested any method or system for manipulating data in a processor, including:

performing a conditional shift operation on an index register ***based on the condition of a carry flag, the condition of the carry flag having been set by a previous arithmetic operation***; and

performing an indexed load operation using an index register. (emphasis added)

as in the present independent claim 1. Analogous features are also contained in the present independent claim 6. In contrast, Cho teaches performing different shift amounts in a load/store instruction *in response to an extension flag, where the extension flag is set responsive to the receipt of* ***an extension instruction,*** *controls access to* ***an extension register,*** *and indicates the* ***active/inactive status of the extension register.*** Cho therefore describes a distinctly different structure and operation from that of the present independent claims 1 and 6, which include the use of a carry flag condition resulting from a previous arithmetic operation as the basis of a conditional shift operation.

The contrast between the extension flag of the Cho system and the features of the present independent claims is clear from many portions of the Cho disclosure. For example, Claim 1 of Cho teaches that the extension flag is set in response to execution of an extension instruction. Claim 7 of Cho teaches that the extension flag controls access to the extension register of the Cho system. And Claim 10 of Cho teaches that the extension flag indicates the active/inactive status of the Cho extension register. Further regarding the extension register, Claim 22 of Cho provides a states as follows:

> . . . an ***extension flag*** which is activated by the extension instruction, wherein, depending on whether the extension flag is activated or inactive (i.e. its value), the instruction decoder and controller decodes the operational code of the extension instruction, to (if during the execution of a first extension instruction the ***extension flag*** is inactive i.e. its value=0), thereby store the operand stored in the operand field of the extension instruction in the extension register as extension data, and activates the ***extension flag***, to thereby use the operand stored in the operand field of the general instruction, or (if during

the execution of a general instruction the extension flag is active i.e. its value=1) use the operationally processed result obtained by operationally processing the extension data stored in the extension register and the operand stored in the operand field of the general instruction, as an operand for execution of the general instruction to deactivate the ***extension flag***. (emphasis added)

Moreover, beginning at line 36 of column 4 of the Specification, Cho states as follows:

Also, according to the invention, the central processing unit having an extension instruction furthermore comprises ***an extension flag*** for representing the status of the extension data field of the extension register, which is one of the status flags, including one or a plurality of bits that a programmer has an access, in which the instruction including the OP code for representing the operation of memorizing the extension data in the extension data field of the extension register and the immediate constant operand is interpreted in the control block to memorize the immediate constant operand in the extension data field of the extension register and executed in the control block to change the status of the ***extension flag***; the extensible instruction including the OP code and the operand field is interpreted into/executed instruction having only the operand field included in the extensible instruction in the control block according to the ***extension flag*** status, or concatenates the operand field included in the extensible instruction to the extension data memorized in the extension data field of the extension register to form a new operand field and is interpreted into instruction having a newly formed operand field which is executed to execute the extensible instruction in the control block and change the ***extension flag*** status. (emphasis added)

At line 57 of Column 8, Cho teaches that a 19th bit of the status register in the Cho system *is the extension flag*, and this 19th bit is subsequently referred to as the "flag" used in the description cited by the Examiner beginning at line 33 of column 10. Applicants further note that Cho includes no reference to a carry flag of any kind.

For the above reasons, Applicants respectfully urge that Cho does not disclose or suggest all the features of the present independent claims 1 and 6. Accordingly, Applicants submit that Cho does not anticipate claims 1 and 6 under 35 U.S.C. 102.

In paragraphs 4 through 18, the Examiner rejected the dependent claims for obviousness under 35 U.S.C. 103, citing certain combinations of Cho with United States patents 6,157,955 of Narad et al. ("Narad et al."), 5,917,821 of Goboyan et al. ("Goboyan et al."), and United States Published Patent Applications numbers 2003/0035430 A1 of Islam et al. ("Islam et al."), and 2002/0174318 of Stuttard et al. ("Stuttard et al."). Applicants respectfully traverse this rejection.

Narad et al. disclose a packet processing system including a policy engine having a classification unit. Goboyan et al. disclose a look-up engine for packet-based network. Islam et al. disclose a programmable network device, and Stuttard et al. disclose a parallel data processing apparatus. None of the combined references include any discussion of a carry flag. Moreover, like Cho, the references cited in combination with Cho in paragraphs 4 through 8 of the Office Action include no teaching or suggestion of any method or system for manipulating data in a processor, including:

> . . .
> performing a conditional shift operation on an index register ***based on the condition of a carry flag, the condition of the carry flag having been set by a previous arithmetic operation***; and
> performing an indexed load operation using an index register. (emphasis added)

as in the present independent claims 1 and 6, from which claims 2-5 and 7- 19 depend.

For the above reasons, Applicants respectfully urge that the combinations of references cited with Cho in paragraphs 4 through 8 of the Office Action do not disclose or suggest all of the features of the present independent claims 1 and 6. Accordingly, the reference combinations in paragraphs 4 through 8 of the Office Action fail to support a *prima facie* case of obviousness under 35 U.S.C. 103 with respect to these independent claims. As to dependent claims 2-5 and

7-19, they each depend from claims 1 and 6, and are respectfully believed to be patentable over the cited references for at least the same reasons.

For these reasons, Applicants respectfully request that the rejections of the Examiner be withdrawn. Reconsideration of all pending claims is respectfully requested.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone the undersigned, Applicants' Attorney at 978-264-6664 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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Date

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